19-1331; Rev 1; 6/98

EVALUATION KIT AVAILABLE

Upstream CATV Driver Amplifier

General Description

The MAX3532 is a programmable power amplifier for use in upstream cable applications. The device outputs up to 62dBmV (continuous wave) through a 1:2 (voltage ratio) transformer when driven with 36dBmV at its input. It features variable gain, which is controlled via a 3-wire digital serial bus and available in 1dB steps. The operating frequency ranges from 5MHz to 42MHz.

The MAX3532 offers three operating modes: high power, low noise, and transmit disable. High-power mode achieves the highest output levels, while low-noise mode achieves the lowest output noise when driving lower output levels. Transmit disable mode places the device in a high-isolation state with minimum output noise, for use between bursts in TDMA systems.

Two power-down modes are also available. Software shutdown mode permits power-down of all analog circuitry while maintaining the programmed gain setting. Shutdown mode disables all circuitry and reduces current consumption below 10µA.

The MAX3532 comes in a 36-pin SSOP package screened for the extended-industrial temperature range (-40°C to +85°C).

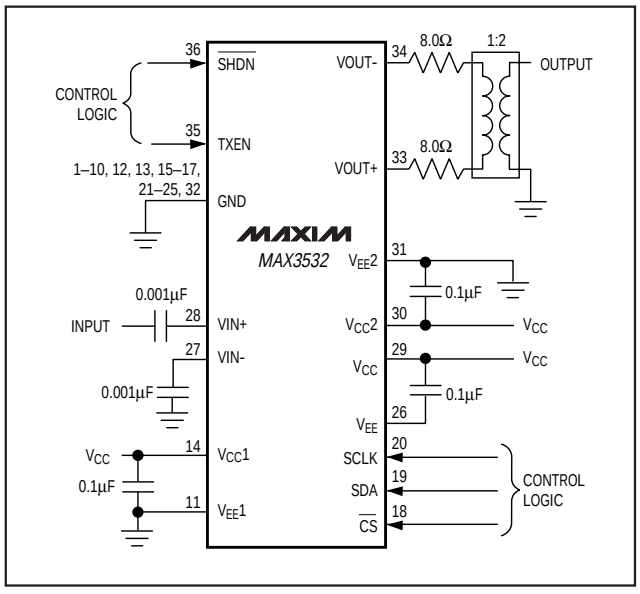
Applications

Cable Modems

Telephony over Cable

CATV Set-Top Box

Typical Operating Circuit



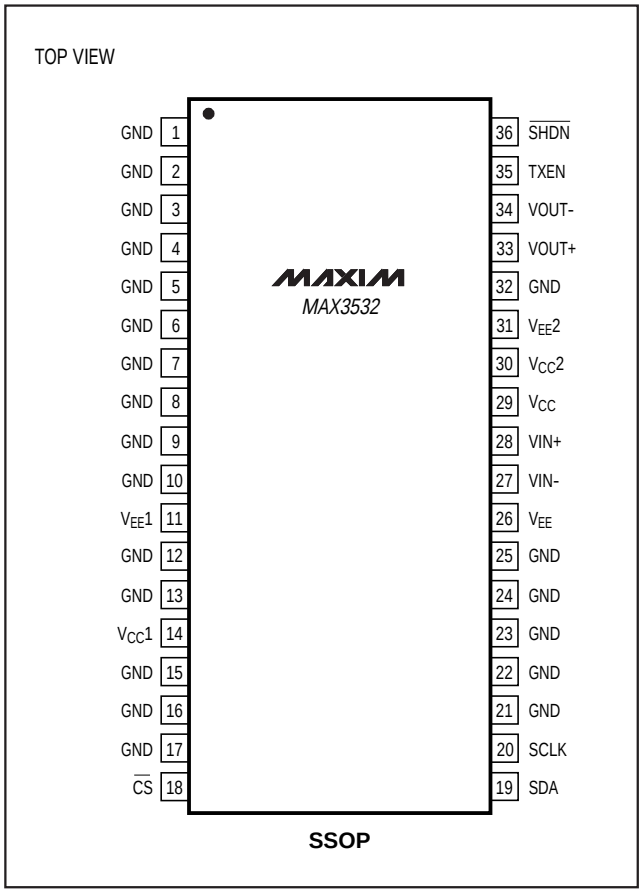
Features

- **Single +5V Supply**
- **Output Level Ranges from Less than 8dBmV to 62dBmV, in 1dB Steps**
- **Gain Programmable in 1dB Steps**
- **350mW Typical Power Dissipation**
- **Transmit-Disable Mode**
- **Two Shutdown Modes**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3532EAX	-40°C to +85°C	36 SSOP

Pin Configuration



†*Protected under U.S. Patent 5,748,027*

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +7.0V
Input Voltage Levels (all inputs).....-0.3V to (V_{CC} + 0.3V)
Continuous RMS Input Voltage (VIN+, VIN-).....60dBmV
Continuous Current (VOUT+, VOUT-).....100mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin SSOP (denote at 11mW/°C above +70°C) 900mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, no RF applied, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75		5.25	V
Supply Current	I_{CC}	TXEN = 1, $\overline{SHDN}$ = 1, D7 and D6 = 1X or 01		75	95	mA RMS
Software Shutdown Current	I_{CC}	TXEN = X, $\overline{SHDN}$ = 1, D7 and D6 = 00		1.5	2	mA
Shutdown Current	I_{CC}	TXEN = X, $\overline{SHDN}$ = 0, D7 and D6 = XX		0.1	10	µA
Digital Input High Voltage	V_{IH}	$\overline{CS}$, SDA, SCLK, TXEN, $\overline{SHDN}$	2.4			V
Digital Input Low Voltage	V_{IL}	$\overline{CS}$, SDA, SCLK, TXEN, $\overline{SHDN}$			0.8	V
Digital Input High Current	I_{IH}	$\overline{CS}$, SDA, SCLK, TXEN, $\overline{SHDN}$			100	µA
Digital Input Low Current	I_{IL}	$\overline{CS}$, SDA, SCLK, TXEN, $\overline{SHDN}$	-100			µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{IN} = 36dBmV, $\overline{SHDN}$ = TXEN = 1, f_{IN} = 20MHz, Z_{LOAD} = 75Ω through a 1:2 transformer with two precision 8.0Ω back-termination resistors, T_A = -40°C to +85°C, unless otherwise noted. Typical values are measured at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Signal Swing	V_{TXOUT}			3.6		Vp-p
Voltage Gain	A_V	High power, D7–D0 = 11111101	24	26		dB
		Low noise, D7–D0 = 1001000		-32	-28	
Output Step Size				1		dB
Isolation in Standby Mode		TXEN = 0, f_{IN} = 42MHz, V_{OUT} = 58dBmV		36		dB
Two-Tone Third-Order Distortion (Note 1)	IMR3	Two input tones at 40MHz and 40.25MHz, both at 30dBmV; V_{OUT} = 52dBmV per tone		-43	-37.5	dBc
Second Harmonic Distortion (Note 1)	HD2	f_{IN} = 20MHz, V_{OUT} = 52dBmV		-59	-55	dBc
		f_{IN} = 20MHz, V_{OUT} = 58dBmV		-46	-40	
Third Harmonic Distortion (Note 1)	HD3	f_{IN} = 14MHz, V_{OUT} = 52dBmV		-67	-58	dBc
		f_{IN} = 14MHz, V_{OUT} = 58dBmV		-57	-48	
AM to AM	AMAM	V_{IN} = 36dBmV to 40dBmV, A_V = 22dB		0.1		dB
AM to PM	AMPM	V_{IN} = 36dBmV to 40dBmV, A_V = 22dB		1		degrees
Output Noise (High-Power Mode) (Note 1)		D7 and D6 = 11, BW = 160kHz, V_{OUT} = 46dBmV to 62dBmV, f = 5MHz to 42MHz		-80	-79	dBc

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{IN} = 36dBmV, $\overline{SHDN}$ = TXEN = 1, f_{IN} = 20MHz, Z_{LOAD} = 75Ω through a 1:2 transformer with two precision 8.0Ω back-termination resistors, T_A = -40°C to +85°C, unless otherwise noted. Typical values are measured at T_A = +25°C.)

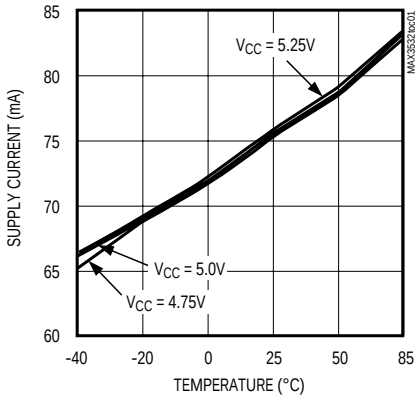
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise (Low-Power Mode) (Note 1)		D7 and D6 = 10, V_{OUT} > 27dBmV, BW = 160kHz, f = 5MHz to 42MHz		-75	-73	dBc
		D7 and D6 = 10, V_{OUT} ≤ 27dBmV, BW = 160kHz, f = 5MHz to 42MHz		-47	-45	dBmV
Output Noise (Standby Mode) (Note 1)		TXEN = 0, BW = 160kHz, f = 5MHz to 42MHz		-47	-45	dBmV
Output Return Loss (Note 1)		f_{IN} = 5MHz to 42MHz	12			dB
TXEN Transient Duration		TXEN rise/fall time < 100ns, T_A = +25°C (Note 1)		3	7	µs
TXEN Transient Step Size		T_A = +25°C, A_V = 22dB (Note 1)		25	100	mV
Power-Enable Transient Duration (Note 1)		T_A = +25°C	1	2.5	5	µs
SERIAL INTERFACE						
$\overline{CS}$ to SCLK Setup Time	$t_{\overline{CSS}}$	(Note 1)	20			ns
$\overline{CS}$ to SCLK Hold Time	$t_{\overline{CSH}}$	(Note 1)	20			ns
SDA to SCLK Setup Time	t_{SDAS}	(Note 1)	20			ns
SDA to SCLK Hold Time	t_{SDAH}	(Note 1)	20			ns
SCLK Pulse Width High	t_{SCLKH}	(Note 1)	50			ns
SCLK Pulse Width Low	t_{SCLKL}	(Note 1)	50			ns

Note 1: Guaranteed by design and characterization.

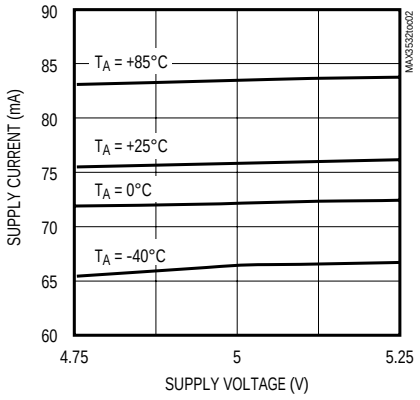
Typical Operating Characteristics

(V_{CC} = 5.0V, V_{IN} = 36dBmV, f_{IN} = 20MHz, $\overline{SHDN}$ = TXEN = 1, Z_{LOAD} = 75Ω through a 1:2 transformer with two precision 8.0Ω back-termination resistors, T_A = +25°C, unless otherwise noted.)

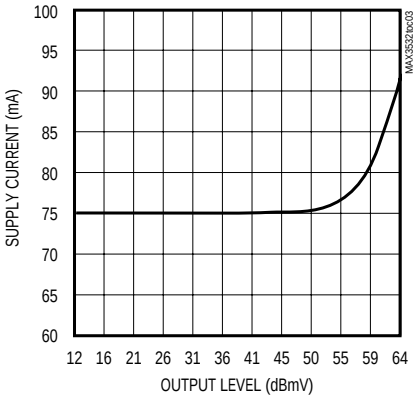
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



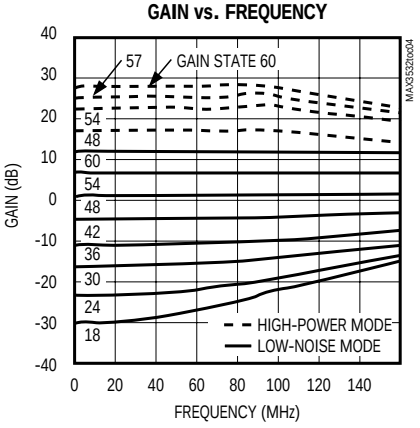
SUPPLY CURRENT vs. OUTPUT LEVEL



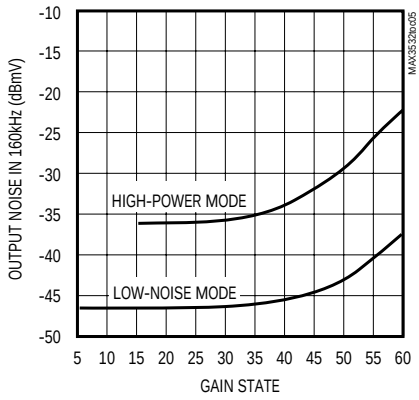
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{IN} = 36dBmV, $\overline{SHDN}$ = TXEN = 1, f_{IN} = 20MHz, Z_{LOAD} = 75Ω through a 1:2 transformer with two precision 8.0Ω back-termination resistors, T_A = -40°C to +85°C, unless otherwise noted. Typical values are measured at T_A = +25°C.)

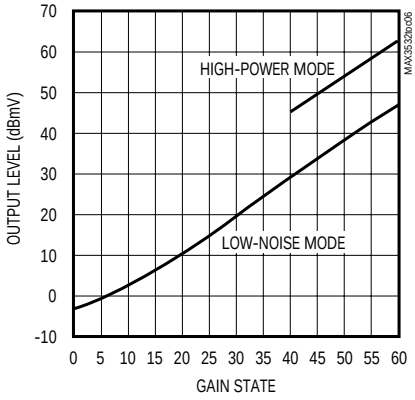
GAIN vs. FREQUENCY



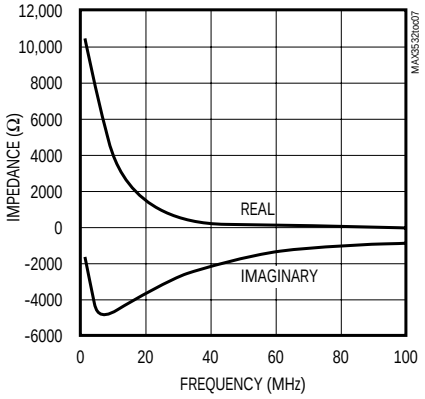
OUTPUT NOISE vs. GAIN STATE



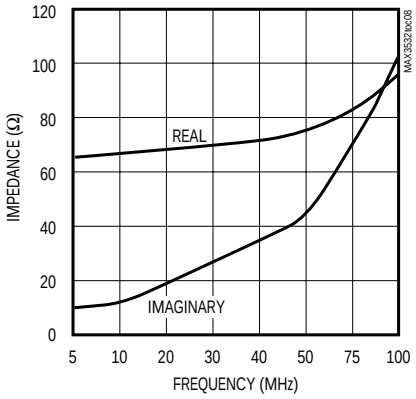
OUTPUT LEVEL vs. GAIN STATE



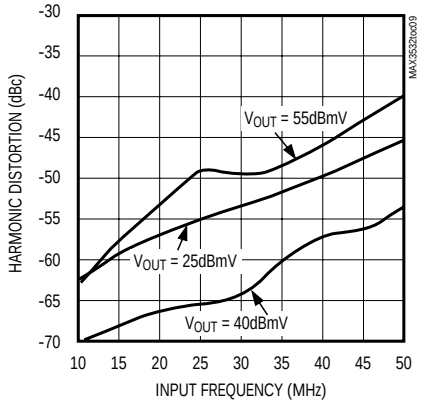
REAL AND IMAGINARY INPUT IMPEDANCE vs. FREQUENCY



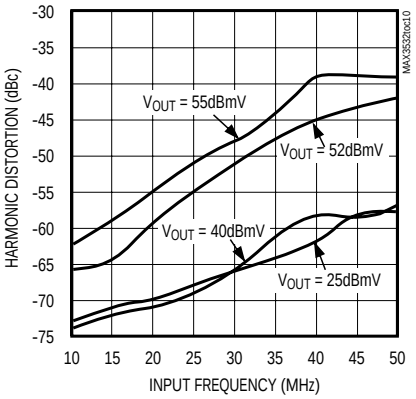
REAL AND IMAGINARY OUTPUT IMPEDANCE vs. FREQUENCY



SECOND HARMONIC DISTORTION vs. INPUT FREQUENCY



THIRD HARMONIC DISTORTION vs. INPUT FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1–10, 12, 13, 15, 16, 17, 21–25, 32	GND	Ground Pins
11	$V_{EE}1$	Serial Data Interface Ground. As with all grounds, maintain the shortest possible (low-inductance) connections to the ground plane.
14	$V_{CC}1$	Serial Data Interface +5V Supply. Bypass this pin with a 0.1µF decoupling capacitor as close to the part as possible.
18	$\overline{CS}$	Serial-Interface Enable. TTL-compatible input. See *Serial Interface* section.
19	SDA	Serial-Interface Data. TTL-compatible input. See *Serial Interface* section.
20	SCLK	Serial-Interface Clock. TTL-compatible input. See *Serial Interface* section.
26	V_{EE}	Programmable Gain Amplifier (PGA) Ground. As with all grounds, maintain the shortest possible (low-inductance) connection to the ground plane.
27	VIN-	Negative Input. When not used, this port must be AC coupled to ground. Along with VIN+, this port forms a high-impedance differential input to the PGA. Driving this port differentially will increase the rejection of second-order distortion.
28	VIN+	Positive Input. Along with VIN-, this port forms a high-impedance differential input to the PGA. Driving this port differentially will increase the rejection of second-order distortion. AC couple to this pin.
29	V_{CC}	PGA +5V Supply. Bypass this pin with a decoupling capacitor as close to the part as possible.
30	$V_{CC}2$	Power Amplifier +5V Supply. Bypass this pin with a decoupling capacitor as close to the part as possible.
31	$V_{EE}2$	Power Amplifier Ground. As with all grounds, connections maintain the shortest possible (low-inductance) length to the ground plane.
33	VOUT+	Positive Output. Along with VOUT-, this pin forms a low-impedance output. Typically this port drives a 1:2 transformer through 8Ω series resistors.
34	VOUT-	Negative Output. Along with VOUT+, this pin forms a low-impedance output. Typically this port drives a 1:2 transformer through 8Ω series resistors.
35	TXEN	Transmit Amplifier Enable. Setting this pin low places the transmitter in a high-isolation state (transmit disable mode). In this mode, however, significant common-mode voltage swings exist. It is, therefore, important to maintain good balance of the differential output through to the transformer primary.
36	$\overline{SHDN}$	Shutdown. When this pin is set low, all functions (including the serial interface) are disabled, leaving only leakage currents to flow.

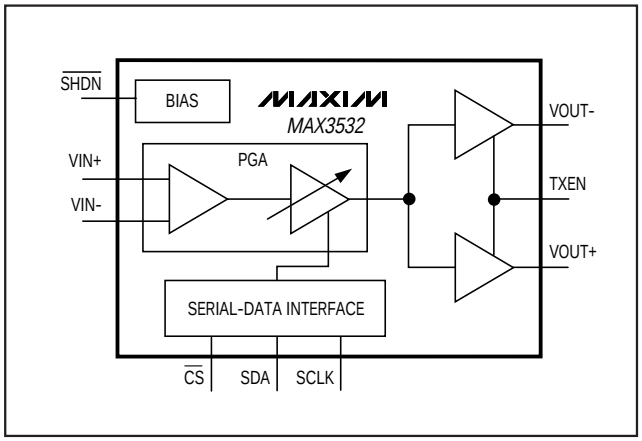


Figure 1. Functional Diagram

Detailed Description

The following sections describe the blocks shown in the Functional Diagram (Figure 1).

Programmable-Gain Amplifier

The MAX3532's processing path is made up of the programmable-gain amplifier (PGA) and the transmit power amplifier, which together provide better than 64dB of output level control in 1dB steps.

The PGA is implemented as a programmable Gilbert cell attenuator. It uses a differential architecture to achieve maximum linearity. When it is driven single ended, specified performance is achieved given that the unused input is decoupled to ground. The gain of the PGA is determined by the serial-data interface. See Table 2.

Transmit Power Amplifier

The transmit power amp is capable of driving +8dBmV to +62dBmV differentially when driven with +36dBmV. To achieve the necessary swing from a single +5V supply, an external 1:2 transformer must be used. The output of the transmit power amplifier is a very low-impedance emitter follower, which requires two 8Ω series termination resistors to achieve adequate output return loss.

The power amplifier's gain is set via the serial-data interface. The transmit power amplifier has a switchable +16dB or +0dB gain to achieve high linearity or low noise, respectively. High-gain mode sets the power amp's gain to +16dB, allowing for the highest output signal swings. Low-noise mode sets the gain to 0dB, which achieves the lowest output noise.

Shutdown Mode

In normal operation the shutdown pin ($\overline{SHDN}$) is driven high. When $\overline{SHDN}$ is asserted low, all circuits within the IC are disabled. Only leakage currents flow in this state. Data stored within the serial-data interface latches will be lost upon shutting down the part.

Transmit-Disable Mode

When the TXEN pin is asserted high, the device is in transmit mode. When TXEN is driven low, the transmit amplifier switches to common-mode operation and the output signal appears at the output pins VOUT+ and VOUT- with the same phase. These identical signals cancel within the output transformer core, providing high isolation from input to output. Optimum isolation is achieved in low-noise mode with a low gain setting.

Serial Interface

The serial interface has an active-low enable ($\overline{CS}$) to bracket the data, with data clocked in MSB first on the rising edge of SCLK. Data is stored in the storage latch on the rising edge of $\overline{CS}$. The serial interface controls the state of the PGA and output amplifier. The register format is shown in Tables 1 and 2. Serial-interface timing is shown in Figure 2.

Transmit Modes

The hardware TXEN line is ANDed with software bit D7, so both TXEN and D7 must be high to transmit. Bit D6 governs whether the device is set to high-gain mode (D6 = 1) or to low-noise mode (D6 = 0). High-power mode should be used for output levels above 45dBmV. This transition point optimizes the MAX3532's distortion performance, but either mode may be used throughout the full complement of programmed gain states. Bits D5–D0 define 64 PGA gain states, nominally 1dB each.

Table 1. Serial-Interface Control Words

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	Chip-State Control MSB
6	D6	Chip-State Control LSB
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

Table 2. Chip-State Control Bits

TXEN	D7	D6	D5	D4	D3	D2	D1	D0	STATE
1	1	1	X	X	X	X	X	X	High-power transmit
1	1	0	X	X	X	X	X	X	Low-noise transmit; subtract 16dB from V_{OUT}
X	0	1	X	X	X	X	X	X	Transmit disabled
0*	X	X							
X	0	0	X	X	X	X	X	X	All analog circuitry off
1	1	0	0	0	1	1	0	1	V_{OUT} = +8dBmV
1	1	0	0	0	1	1	1	0	V_{OUT} = +9dBmV
—	1	—	—	—	—	—	—	—	—
1	1	1	1	1	0	1	0	1	V_{OUT} = +56dBmV
1	1	1	1	1	0	1	1	0	V_{OUT} = +57dBmV

**Except state 000XXXXXX, which is software shutdown.*

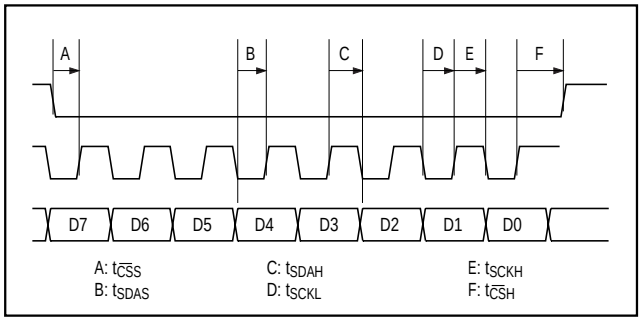


Figure 2. Serial-Interface Timing Diagram

Software Shutdown Mode

Software-shutdown mode is enabled when both D7 and D6 are low (D7, D6 = 00). This mode minimizes current consumption while maintaining the programmed gain state stored in the serial data-interface's latch. All analog functions are disabled in this mode.

Applications Information

Output Match

The MAX3532's output circuit is a differential emitter follower that has a near-zero impedance over the operating frequency range. In order to match to a single-ended impedance, a transformer and back-termination resistors are required. Furthermore, operation from a single +5V supply requires that the output signal swing be stepped up to achieve the rated output levels. These are described in the next two sections.

Transformer

To achieve the rated output levels, a 1:2 (voltage ratio) transformer is required. This transformer must have adequate bandwidth to cover the intended application. Note that most RF transformers specify a bandwidth with a 50Ω load on the primary and a matching resistance on the secondary winding. The much lower (approximately 16Ω due to the back-termination resistors) impedance of the MAX3532's output will tend to shift the low-frequency edge of the bandwidth specification down by a factor of three or more due to primary inductance. Keep this in mind when specifying a transformer.

RF transformer cores are inherently nonlinear devices, which must be operated in their linear region if distortion is a critical consideration. In general, the size of the transformer core used and the number of turns will govern the distortion performance of the transformer for a given output level. Therefore a transformer of adequate size must be used to minimize its contribution to the overall distortion budget.

Back-Termination Resistors

The value of the back-termination resistors depends on two parameters: the ultimate output impedance (as referred through the output transformer), and the quality of the output match desired. The output impedance depends on the value of the termination resistors by the following formula:

$$Z_{OUT} = 4 \times [\, 2 \times (R_{term} + R_P)]$$

where R_{term} is the value of one termination resistor and R_P is parasitic resistance.

Some allowance must be made for parasitic inductance in the transformer as well as on the printed circuit board. Therefore, choose a resistance value lower than a perfect match. Two 8.0Ω resistors will provide a near-optimum match.

If the output match is less than critical, the back-termination resistors can be set to a lower value. This will extend the upper limit of the output level range (by dropping less voltage across the resistors and more across the load), and may improve distortion performance for a given output level.

Layout Issues

A well designed printed circuit board is an essential part of an RF circuit. For best performance pay attention to power-supply layout issues, as well the output circuit layout.

Output Circuit Layout

The differential implementation of the MAX3532's output has the benefit of significantly reducing even-order distortion, the most significant of which is second-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. It is critical that the traces leading from the output pins be exactly the same length.

Since the MAX3532 has a low-impedance output, the output traces must also be kept as short as possible, as small amounts of inductance can have an impact at higher frequencies. The back-termination resistors should be kept as close to the device as possible.

Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large valued decoupling capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the MAX3532 circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local V_{CC} decoupling at each V_{CC} pin.

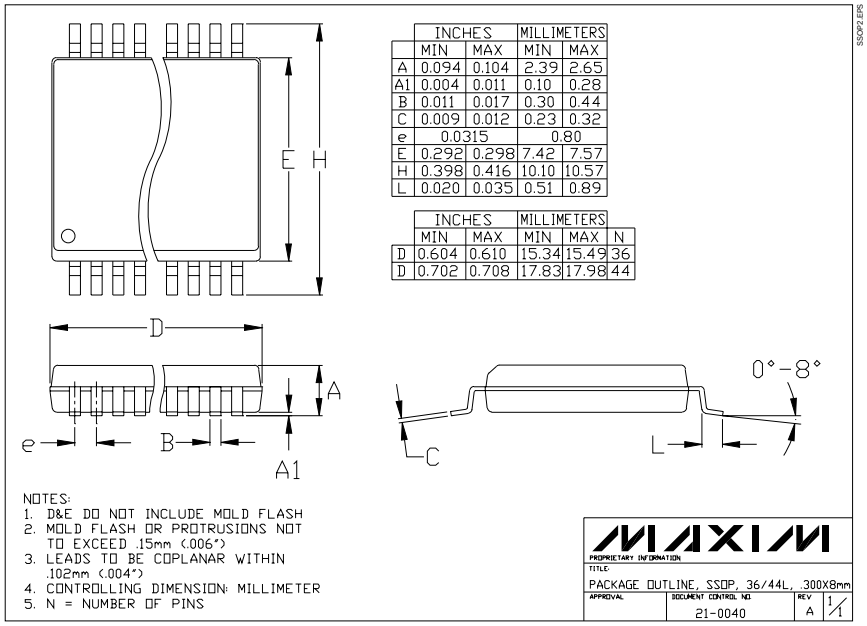
The traces leading from the supply to V_{CC} (pin 29) and $V_{CC}2$ (pin 30) must be made as thick as practical to keep resistance well below 1Ω.

Ground inductance degrades distortion performance. Therefore, ground plane connections to V_{EE} (pin 26) and V_{EE2} (pin 31) should be made with multiple vias if possible.

Chip Information

TRANSISTOR COUNT: 1100

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44